CLAIMS

What is Claimed is:

1. A computer system including a circuit board, said computer system comprising:

a first slot and a second slot coupled to said circuit board, said first slot including a first connector and said second slot including a second connector, said first and second connectors each having a column and row arrangement of connector-pins, said first connector including first, second and third connector-pins and said second connector including fourth, fifth and sixth connector-pins;

first, second, third, fourth, fifth and sixth signal lines connected to said first through sixth connector-pins, respectively;

a primary hot swap controller having a first means for simultaneously turning on/off a first plurality of switches, a second means for driving signal lines connected to said first, second, fourth, and fifth connector-pins, and a third means for storing a status information of said signal lines;

a backup hot swap controller having a fourth means for simultaneously turning on/off a second plurality of switches, a fifth means for driving said signal lines connected to said first, second, fourth, and fifth connector-pins and for storing a status information of said signal lines,

wherein, during a normal operation of said computer system, said first means turns on said first plurality of switches such that said second means drives said signal lines connected to said first, second, fourth, and fifth connector-pins and said fourth means turns off said second plurality of switches, and during a backup operation of said computer system, said first means turns off said first plurality of switches and said fourth means turns on said second plurality of switches such that said fifth means drives said signal lines connected to said first, second, fourth, and fifth connector-pins according to said status information stored in said fifth means.

2. The computer system of Claim 1, wherein said primary hot swap controller includes a first communication control circuit, said second means connected to said first plurality of switches and to said first means, said first means connected to activation terminals of said first switches via a first control line so as to simultaneously turn on/off said first plurality of switches, said communication control circuit connected to said first means, and said first through sixth connector-pins connected to said second means via said signal lines and through respective ones of said first plurality of switches.

3. The computer system of Claim 2, wherein said fifth means is connected to said second plurality of switches and to said fourth means, said fourth means is connected to respective activation terminals of said second switches via a second control line so as to simultaneously turn on/off said second plurality of switches, said fourth means having a communication link with said first communication control circuit, and said first through sixth connector-pins connected to said fifth means via said signal lines and through respective ones of said second plurality of switches.

4. The computer system of Claim 1, wherein said first means includes an arbitration control circuit, said second means includes a core control circuit, and said third means includes a first register.

5. The computer system of Claim 1, wherein said fourth means includes a second communication control circuit, said fifth means includes a second register.

6. The computer system of Claim 3, wherein said communication link connecting said first communication control circuit and said fourth means comprise an asynchronous communication link.

7. The computer system of Claim 6, wherein said asynchronous communication link includes a data line and a clock line.

8. The computer system of Claim 3, wherein said communication link connecting said first communication control circuit and said fourth means comprise a synchronous communication link.

9. The computer system of Claim 8, wherein said synchronous communication link includes a plurality of data lines, a plurality of control lines, and a select/strobe control line.

10. The computer system of Claim 2, wherein during every programmed interval of said normal operation, the status of said signal lines connected to said first through sixth connector-pins are transmitted from said first communication control circuit to said fourth means and stored in said fifth means.

11. The computer system of Claim 2, wherein said first communication control circuit is connected to said first means via a plurality of control lines.

12. The computer system of Claim 1, wherein said first means is connected to said second means via a plurality of control lines.

13. The computer system of Claim 1, wherein said fourth means is connected to said fifth means via a plurality of signal lines.

14. A hot swappable computer system including a circuit board, said circuit board having a slot with a first connector, said first connector having connector-pins in a column and row arrangement and including first, second and third connector-pins, said computer system comprising:

first, second and third signal lines connected to said first, second, and third connector-pins, respectively;

a primary hot swap controller having a core control circuit including a first register, a plurality of first switches, a first communication control circuit, and an arbitration control circuit, said core control circuit connected to said plurality of first switches and said arbitration control circuit, said arbitration control circuit connected to said first communication control circuit and to activation terminals of said first switches via a common control line such that said first switches are turned on/off simultaneously by said arbitration control circuit;

a backup hot swap controller having a second register, a plurality of second switches, and a second communication control circuit, said second register connected to said second switches and said second communication control circuit, said second communication control circuit connected to respective activation terminals of said second switches via a common control line such that said second switches are turned on/off simultaneously by said second communication control circuit, and said second communication control circuit has a communication link with said first communication control circuit,

wherein during a normal operation of said computer system, said primary hot swap controller drives said first, second, and third signal lines, and during a backup operation of said computer system said backup hot swap controller drives said first, second, and third signal lines according to a status of said respective signal lines stored in said second register.

15. The computer system of Claim 14, wherein said communication link connecting said first and second communication control circuits comprise an asynchronous communication link.

16. The computer system of Claim 15, wherein said asynchronous communication link includes a data line and a clock line.

17. The computer system of Claim 14, wherein said communication link connecting said first and second communication control circuits comprise a synchronous communication link.

18. The computer system of Claim 17, wherein said synchronous communication link includes a plurality of data lines, a plurality of control lines, and a select/strobe control line.

19. The computer system of Claim 14, wherein during every programmed interval of said normal operation, the status of said signal lines connected to said first through third connector-pins are transmitted from said first communication control circuit to said second communication control circuit and stored in said second register.

20. The computer system of Claim 14, wherein said first register stores a status of said first, second, and third signal lines.

21. The computer system of Claim 14, wherein said arbitration control circuit is connected to said first communication control circuit via a plurality of control lines.

22. The computer system of Claim 14, wherein said arbitration control circuit is connected to said core control circuit via a plurality of control lines.

23. The computer system of Claim 14, wherein said second communication control circuit is connected to said second register via a plurality of signal lines.

24. A backup hot swap controller for use in a hot swappable computer system including a circuit board having slots with connectors having a column and row arrangement of connector-pins, first ones of said connectors of said slots having first, second and third connector-pins, said backup hot swap controller comprising:

a plurality of switches, respective ones of said plurality of switches connected to said first, second, and third connector-pins via signal lines;

a register for storing status information of said signal lines, and said register connected to said plurality of switches; and

a communication control circuit connected to said register, said communication control circuit connected to respective activation terminals of said switches and having a common control line for simultaneously turning on/off of said plurality of switches;

wherein during a period when said communication control circuit turns on said switches, said register drives said signals lines connected to said first, second and third connector-pins according to said status stored in said register.